REMARKS

Claims 1-8 and 10-19 are currently active.

Antecedent support for the amendments to the claims is found on page 9, lines 14-18.

The Examiner has rejected Claims 1-8 as being unpatentable over Suzuki in view of Azevedo. Applicants respectfully traverse this rejection.

Suzuki teaches a data transfer system which can make a stable communication without causing erroneous operations when a communication is resumed after suspension due to an abnormal state such as a power failure. See column 2, lines 17-22. Abnormal circumstances may include a power failure, a momentary power failure, and hang up or the like. See column 2, lines 32-35.

Suzuki teaches a data transfer system employing a bus, a master device 1 composed of a microcomputer and a plurality of slave devices 2.

The master device has a terminating function which transmits a stop condition as signals for terminating communication to the slave devices in order to terminate communication at the time of the occurrence of abnormal circumstances during communication. A master device also has a resuming function which transmits a start condition as signals for resuming communication to the slave devices after transmitting a stop condition at the time abnormal circumstances are resolved.

At the time of an occurrence of abnormal circumstances, the master device detects variations of a power source voltage, and determines that an abnormal circumstance such as a power failure, a momentary power failure and the like occurs when the power source voltage decreases below a predetermined value. Subsequently, the master device transmits a stop condition to the slave device in transit, and terminates communication. See column 3, lines 30-50.

The slave device operates to suspend communication upon receipt of the stop condition, thereby ensuring that a data transfer suspended by the master device is not continued at the slave device. Although a power voltage is gradually decreased due to an interruption of power supply, the slave device is operable for a certain period after the occurrence of a power failure since a power supply voltage for stopping the slave device is considerably low. Accordingly, the slave device can receive the stop condition from the

master device within this period. When a power supply is resumed after resolving a power failure, the master device detects a power voltage and determines that a normal state is recovered, and then starts to operate. In case the master device is suspended due to the occurrence of abnormal circumstances, the operation is resumed by inputting reset signals. See column 3, line 60-column 4, line 3.

Claim 1 of applicants has the limitation of "the master unit having a software program causes the master unit to automatically recover and restart when a slave unit fails which has caused the master unit to fail and to avoid further accessing the failed slave unit." It is respectfully submitted that Suzuki does not teach or even suggest this limitation. As explained above, Suzuki is focusing on some form of a power failure and certainly does not teach or suggest anywhere the very specific event of a slave unit failing which causes the master unit to fail. In fact, from the teachings of Suzuki, it is clear that the slave unit does not fail and must be sent a stop condition since power voltage is gradually decreased due to an interruption of power supply and the slave device is operable for a certain period after the occurrence of a power failure since the power supply voltage for stopping the slave device is considerably low. Thus, not only does Suzuki fail to teach or suggest that it is the slave unit which fails which causes the master unit to fail, but one of the key teachings of Suzuki is for a stop condition to be transmitted to the slave device so no faulty data is received and processed by the slave device which has remained active.

Additionally, Suzuki does not teach or suggest that the master unit avoids further accessing the failed slave unit. Suzuki simply teaches that a stop condition is sent to the slave device and after the power failure is resolved, communication is resumed to the slave device. See column 4, line 11.

The Examiner recognizes that Suzuki fails to teach a slave device failure. To attempt to overcome this deficiency, the Examiner cites Azevedo for teaching this limitation of applicants' claimed invention. However, applicants respectfully submit that Azevedo also fails to teach or suggest a slave device failure as claimed by applicants. Specifically, applicants' claimed invention has the limitation of "a software program that causes the master unit to automatically recover and restart when a safe unit fails which has caused the master unit to fail and to avoid further accessing the failed slave unit". Azevedo does not teach a slave unit fails, or a slave unit fails which could cause the master unit to fail or to avoid further accessing the failed slave unit, or to automatically recover and restart the master unit.

Applicants have carefully used their language to describe their claimed invention, as it is well recognized that applicants are the lexicographers regarding their invention. Applicants have used the term "fail" and used the term "restart" as accepted well-recognized language to describe the claimed invention. Instead, Azevedo teaches not a failure, but a hang, and not at all to restart, but to reset. This is important, because what Azevedo is directed to and

the teachings all describe is a situation where there has been no failure, but that the master has always continued its operation; that is, it has never failed, so it does not have to restart. To restart a system that has failed is materially different and distinct and more complex than a system that is never stopped working.

More specifically, Azevedo teaches shared bus hang conditions may occur in the multi-master communication system for various reasons. A bus hang condition may or can happen due to an unrecognized address on the shared bus, when the bus master cannot abort the transfer on the shared bus. The shared bus could hang if a request for transfer via the external bus was not granted in time by the bus adapter, and the buffer becomes full, or if a deadlock occurred between the host processor on the external bus in the master on the shared bus. Further, a hang state could occur if no slave acknowledged an address issued on the shared bus, or if there was a hardware problem. If a hang condition occurred on the shared bus, it may have locked the processor, if it was processing an operation which needed the shared bus to complete. Thus, the subsystem processor may be unable to proceed see column 7, lines 1-20. Thus, it is clear from all these teachings that Azevedo is directed to the actual transfer of data or the inability to complete the transfer when it is talking about a hang condition, and not at all to do with a failure. It should be emphasized that what makes it clear the failure is different from a hang condition is taught by Azevedo is also the use of the term "restart" in applicants' claimed invention.

Azevedo teaches that the shared bus hang prevention and recovery method and the hang prevention device embodiments can be used to prevent a permanent bus hang condition and to allow recovery of the subsystem to a known state, such as reset state. The hang prevention device is used to monitor the shared bus and provide a way to interrupt any transfer in progress causing the hangup. It also provides the information necessary for recovery and problem determination. See column 7, lines 40-49. Again, from this teaching, it is clear that Azevedo is focusing on the transfer event and monitoring" controlling such a transfer. It teaches the ability to interrupt any transfer causing the hangup. Nowhere is there any teaching or suggestion of a failure or a restart, which, as explained above, is distinct from a hang condition.

In addition, Azevedo does not teach or suggest "to avoid further accessing the failed slave unit". Azevedo specifically teaches to not grant further access to the master attached to the external bus to prevent further bus hang ups before the subsystem is reset. That is, after a reset, further access is allowed. It must also be emphasized that what Azevedo is teaching his access to the external bus and is not at all talking about a failed slave unit. This is contrary to applicants' claimed invention. Accordingly, Claim 1 of applicants is not made obvious by Suzuki and Azevedo.

Claims 2-5 are patentable for the reasons Claim 1 is patentable.

Claim 6 is patentable for the reasons Claim 1 is patentable.

Claim 7 is dependent to parent Claim 6 and is patentable for the reasons Claim 6 is patentable.

Claim 8 is patentable for the reasons Claim 1 is patentable.

The Examiner has rejected Claims 10-19 as being unpatentable over Suzuki in view of Azevedo and Cepulis. Applicants respectfully traverse this rejection. Cepulis has been previously discussed in combination of a previous rejection with Abramson, that was overcome prior to this Office Action. As explained above, Suzuki and Azevedo fail to teach or suggest the limitation of "determining a master unit abnormally terminated when the master unit attempted to access a first slave unit which caused the master unit to fail". Cepulis also fails to teach or suggest this limitation. The Examiner cites Cepulis simply for the supposed teaching that the master unit is directed to avoid further accessing the failed slave unit. Accordingly, Claim 8 is patentable over the applied art of record. Claims 10-19 are dependent to parent Claim 8 and are patentable for the reasons Claim 8 is patentable.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1-8 and 10-19, now in this application be allowed.

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